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Introduction To FPGA And CPLD – Lesson 3: Input and Output

HOMEWORK

The following homework questions are meant to go with the online lesson found here:

http://www.pyroelectro.com/edu/fpga/input_output/

The homework for this course will follow a very simple format. Each course will have a homework download for you to do offline and it will consist of 3-5 questions that you should be able to answer if you watched the course.

The questions are not meant to be so challenging as to take you hours to finish, but to stress the more important parts of the lessons and get you thinking about what they mean and how you understand them.

I highly encourage you to post your answers to homework questions in the forums so you can double check that you are getting the right theoretical and practical understanding from the lessons and so that we can start fun conversations about electronics!

HOMEWORK QUESTION 1

How do you define a 1 bit logic input in a top level entity in VHDL? What about a 1 bit logic output?

HOMEWORK QUESTION 2

Which input/output logic levels is the EPM3032A CPLD compatible with?

HOMEWORK QUESTION 3

What is the purpose of the 10kΩ pull down resistor connected to the push-button? What do you think would happen if it wasn't there?

ADDITIONAL INFORMATION

To get feedback on your homework or to ask additional questions related to this lesson, please post your homework answers or your questions in the online forums at:

<http://www.pyroelectro.com/forums/viewforum.php?f=26>