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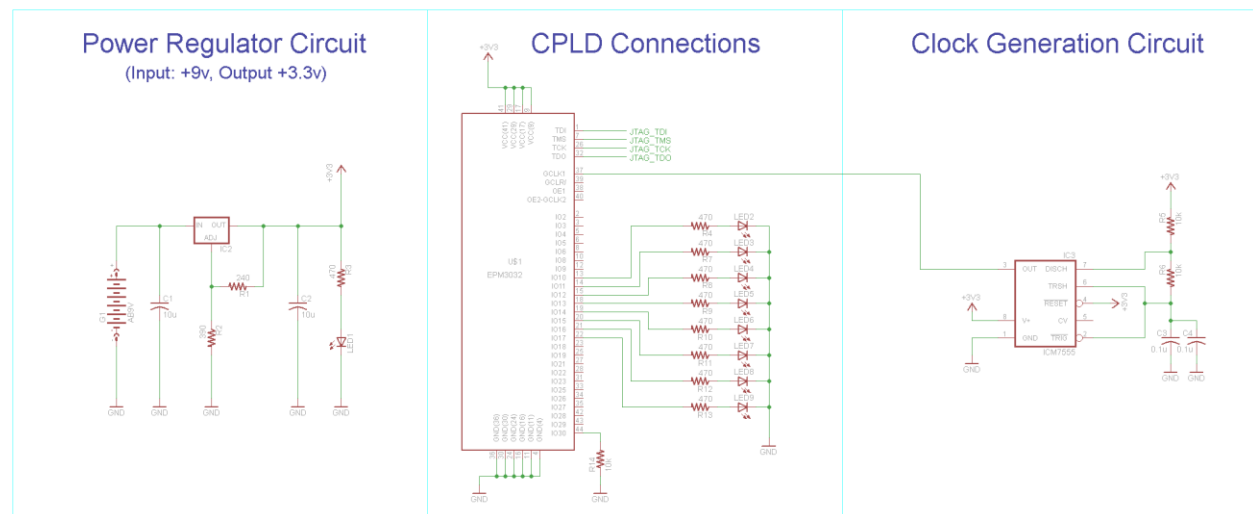
## Introduction To FPGA And CPLD – Lesson 9: Handheld LED POV

### SCHEMATICS

The following schematic material is meant to go with the online lesson found here:  
[http://www.pyroelectro.com/edu/fpga/handheld\\_pov/](http://www.pyroelectro.com/edu/fpga/handheld_pov/)

### LESSON9 HARDWARE SCHEMATIC

In lesson 9 we simply took the lesson 8 schematic, added 4 more resistors and LEDs to the CPLD and modified the clock generation circuit's two capacitors so that they are in parallel instead of in series. Here is the full schematic:



Putting the two capacitors in parallel makes the effect capacitance 0.2uF which creates a clock output to the CPLD of about 250 Hz. A good POV should run at about 100-150 Hz, so we'll divide it down by 2 inside of the CPLD.

### ADDITIONAL INFORMATION

To ask questions about anything found in this schematic please head on over to the forums located at:

<http://www.pyroelectro.com/forums/viewforum.php?f=26>