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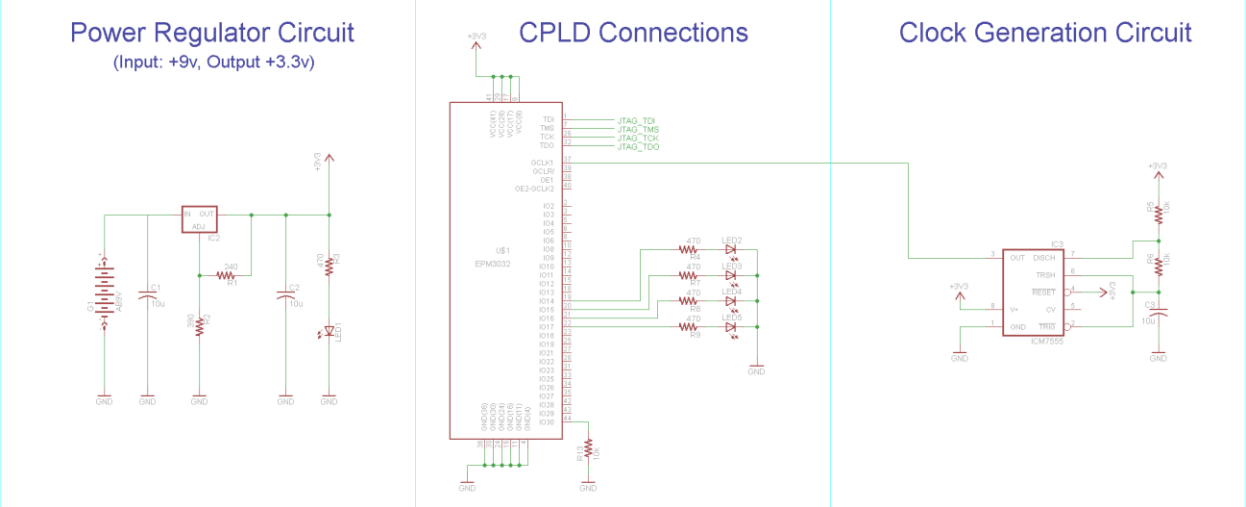
Introduction To FPGA And CPLD – Lesson 10: VHDL vs Verilog vs Schematic

SCHEMATICS

The following schematic material is meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/vhdl_verilog_schematic/

LESSON10 HARDWARE SCHEMATIC

In lesson 10 we build the hardware counter/timer circuit again and used 3 different methods of creating the code for the CPLD, VHDL/Verilog/Schematic. The focus of this lesson was the cpld image side, not the hardware, so the schematic is very simple. Here's the full schematic:



This circuit uses the ICM7555 timer to generate a +3.3v clock signal at a slow 10-15 Hz frequency for the CPLD to use as a timer. All power voltages used are +3.3v coming from the regulator circuit.

ADDITIONAL INFORMATION

To ask questions about anything found in this schematic please head on over to the forums located at:
http://www.pyroelectro.com/forums/viewforum.php?f=26