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Introduction To FPGA And CPLD – Lesson 10: VHDL vs Verilog vs Schematic

HOMEWORK

The following homework questions are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/vhdl_verilog_schematic/

The homework for this course will follow a very simple format. Each course will have a homework download for you to do offline and it will consist of 3-5 questions that you should be able to answer if you watched the course.

The questions are not meant to be so challenging as to take you hours to finish, but to stress the more important parts of the lessons and get you thinking about what they mean and how you understand them.

I highly encourage you to post your answers to homework questions in the forums so you can double check that you are getting the right theoretical and practical understanding from the lessons and so that we can start fun conversations about electronics!

HOMEWORK QUESTION 1

Which design methodology (Verilog / VHDL / Schematic) is best suited for a large scale project? Why?

HOMEWORK QUESTION 2

Use the schematic – block diagram design method to make a simple design of your choice.

HOMEWORK QUESTION 3

After getting a sneak peak at Verilog, VHDL and Schematic. Which method of building a CPLD/FPGA image do you like the most? Why?

ADDITIONAL INFORMATION

To get feedback on your homework or to ask additional questions related to this lesson, please post your homework answers or your questions in the online forums at:
http://www.pyroelectro.com/forums/viewforum.php?f=26