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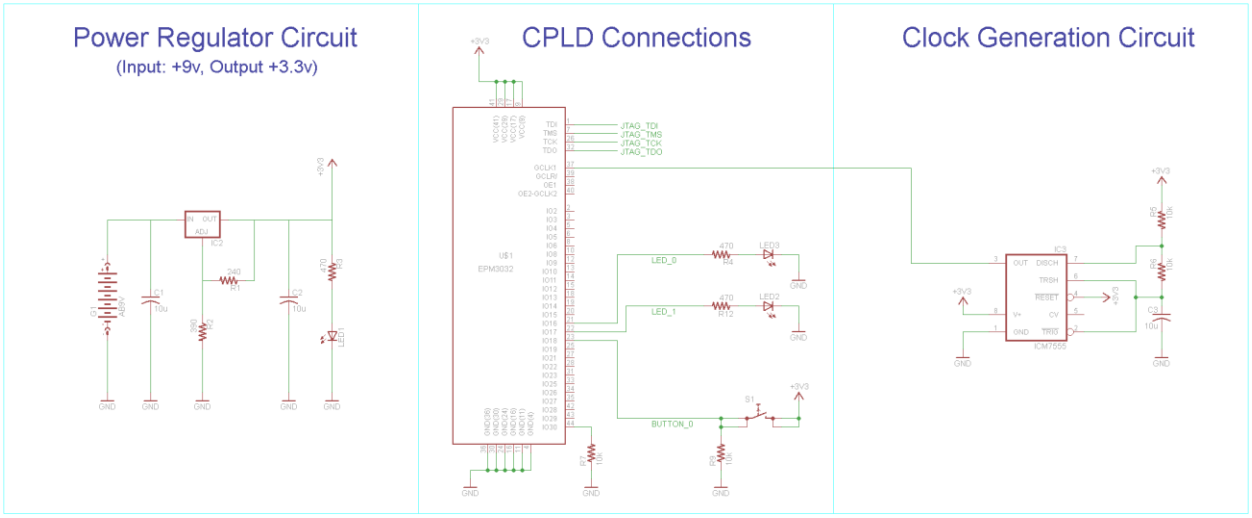
Introduction To FPGA And CPLD – Lesson 5: Procedural Logic

SCHEMATICS

The following schematic material is meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/procedural_logic/

LESSON5 HARDWARE SCHEMATIC

Lesson5 showed us how we could use the CPLD to make our own custom D-Flip-Flop. The circuit for this lesson was fortunately not too different from lesson4, so it should be easy to follow. Below is the schematic for this lesson:



This schematic shows 1 input from a push buttons and 2 output to an LEDs all connected to the CPLD. The big new addition is the ICM7555 clock circuit, which outputs a 10-15 Hz clock signal to the CPLD.

ADDITIONAL INFORMATION

To ask questions about anything found in this schematic please
head on over to the forums located at:
http://www.pyroelectro.com/forums/viewforum.php?f=26