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*Introduction To FPGA And CPLD – Lesson 5: Procedural Logic*

FORMULAS

The following formulas and information are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/procedural_logic/

## LESSON5 VHDL CODE

In lesson 5 we created out own D-flip-flop logic element using VHDL with the customization that it also had a clock divide by 2 output.

The VHDL code for this project can be seen in the box to the right. You can copy and paste it easily into Quartus II for compilation but I implore you to read through and understand what each line does before doing so.

Comments were used in the entity declaration to show which pins should be connected to which I/O's on the CPLD.

**Lesson5.vhd**

```
library ieee;
use ieee.std_logic_1164.all;

entity lesson5 is
    port(
    RESET:  in std_logic; --PIN_44
    CLOCK:  in std_logic; --PIN_37
    BUTTON_0:in std_logic; --PIN_23
    LED_0:  out std_logic; --PIN_21
    LED_1:  out std_logic
    );
end lesson5;

architecture rtl of lesson5 is

signal blink: std_logic;
signal data: std_logic;

begin

    DATA_REGISTER_0: process(RESET, CLOCK,
BUTTON_0)
    begin
        if RESET = '1' then
            data <= '0';
            blink <= '0';
        elsif rising_edge(CLOCK) then
            data <= BUTTON_0;
            blink <= not blink;
        end if;
    end process DATA_REGISTER_0;

    LED_0 <= blink;
    LED_1 <= data;

end rtl;
```

## ADDITIONAL INFORMATION

If you have any questions about the formulas or information found in this document, please feel free to head on over to the forums and ask us some questions!
http://www.pyroelectro.com/forums/viewforum.php?f=26