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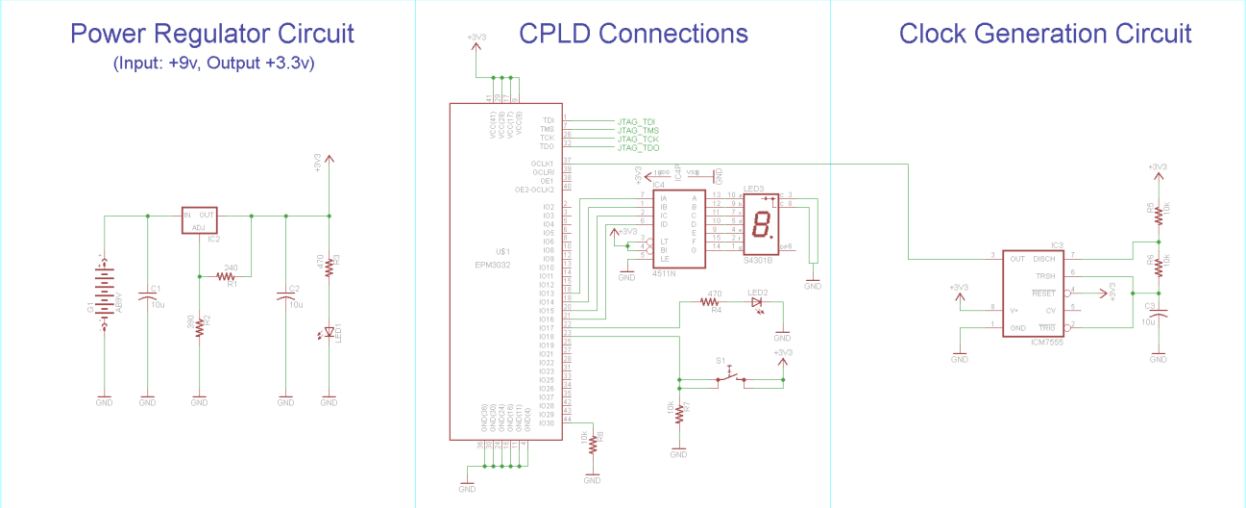
Introduction To FPGA And CPLD – Lesson 7: Parallel Hardware

SCHEMATICS

The following schematic material is meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/parallel_hardware/

LESSON7 HARDWARE SCHEMATIC

In lesson 7 we built two hardware modules in one CPLD. The first was a timer-counter that counted up outputting a 4-bit value with each count. A 7 segment display output the current value in decimal. We also had a basic d-flip-flop with a push button input and red led output. Here's the full schematic:



This schematic is a little more complicated than the other lesson, but the end result shows you how CPLDs and FPGAs are capable of complex and independent hardware modules inside of one configurable device.

ADDITIONAL INFORMATION

To ask questions about anything found in this schematic please head on over to the forums located at:
http://www.pyroelectro.com/forums/viewforum.php?f=26