PyroElectro.com - PyroEDU

Introduction To FPGA And CPLD – Lesson 7: Parallel Hardware

HOMEWORK

The following homework questions are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/parallel_hardware/

The homework for this course will follow a very simple format. Each course will have a homework download for you to do offline and it will consist of 3-5 questions that you should be able to answer if you watched the course.

The questions are not meant to be so challenging as to take you hours to finish, but to stress the more important parts of the lessons and get you thinking about what they mean and how you understand them.

I highly encourage you to post your answers to homework questions in the forums so you can double check that you are getting the right theoretical and practical understanding from the lessons and so that we can start fun conversations about electronics!

HOMEWORK QUESTION 1

What are some advantages of building CPLD hardware modules that operate in parallel?

HOMEWORK QUESTION 2

Create a new CPLD project and build two combinatorial logic statements that operate in parallel: Y = (A + BC) , Z = (D + E + F). Show the RTL viewer output to prove they will be parallel statements.

HOMEWORK QUESTION 3

In lesson 7 we gave an example of bit-coin mining, where a CPLD/FPGA would out-perform a processor. Can you think of another example?

ADDITIONAL INFORMATION

To get feedback on your homework or to ask additional questions related to this lesson, please post your homework answers or your questions in the online forums at:
http://www.pyroelectro.com/forums/viewforum.php?f=26