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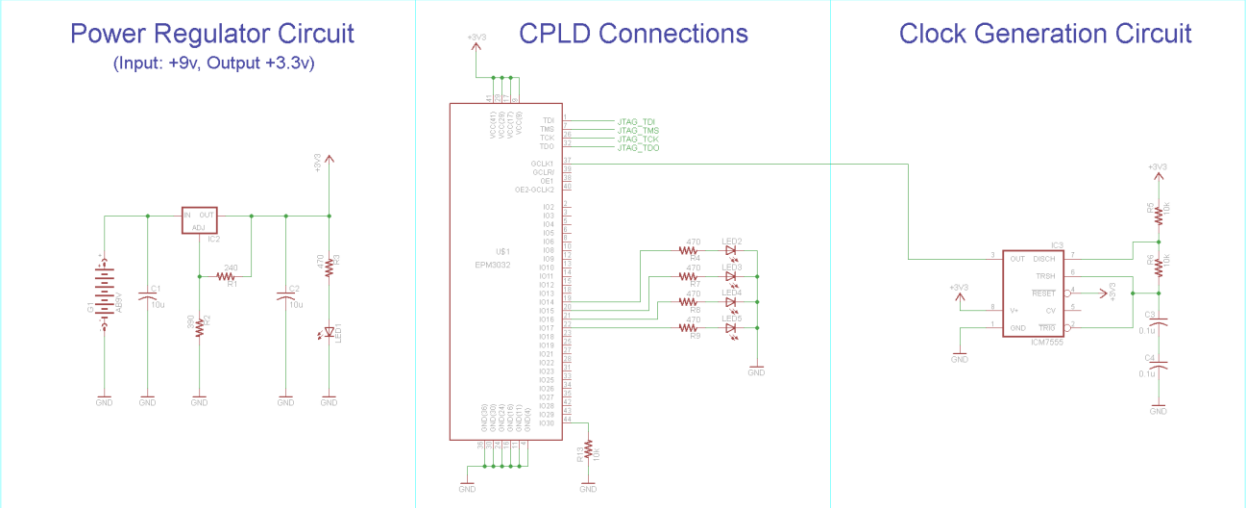
Introduction To FPGA And CPLD – Lesson 8: LED Dimming via PWM

SCHEMATICS

The following schematic material is meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/led_dimming_pwm/

LESSON8 HARDWARE SCHEMATIC

In lesson 8 we built a row of LEDs that faded in using the power of digital PWM. The hardware schematic only changed a little compared to previous lessons with a different clock generation circuit output frequency and using 4 LEDs connected to the CPLD. Here is the complete schematic:



The two 0.1uF capacitors used in the clock generation circuit are connected in series. This makes the effective capacitance at pins 2 & 6 actually around 0.05uF which allows our clock output to be around 900-1,000 Hz.

ADDITIONAL INFORMATION

To ask questions about anything found in this schematic please
head on over to the forums located at:
http://www.pyroelectro.com/forums/viewforum.php?f=26