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Introduction To FPGA And CPLD – Lesson 8: LED Dimming via PWM

FORMULAS

The following formulas and information are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/led_dimming_pwm/

LESSON8 VHDL CODE

In lesson 8 we built a basic PWM output module that varied the PWM output by 6.25% every 100 clock cycles.

This was achieved by using a fast timer-counter found in the PWM_MODULE_0 and a slow timer-counter found in the COUNTER_0 module.

The fast timer kept track of the complete period cycle as well as when the outputs should be a logic ‘1’ or ‘0’.

The slower timer was used to increment the count_1 value for telling the PWM_MODULE_0 how long the led outputs should remain at logic ‘1’ and logic ‘0’.

When these two processes are combined together, we get a slowly incrementing PWM output that when it over flows at 100% bright resets to 0% and starts all over again.

Lesson8.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity lesson8 is
   port(
   RESET:  in std_logic;
   CLOCK_0: in std_logic;
   LED:      out std_logic_vector(3 downto 0)
   );
end lesson8;

architecture rtl of lesson8 is

signal count_0 : std_logic_vector(3 downto 0);
signal count_1 : std_logic_vector(3 downto 0);
signal led_output : std_logic_vector(3 downto 0);

begin
      PWM_MODULE_0: process(RESET,CLOCK_0)
      begin
         if RESET = '1' then
            count_0 <= "0000";
         elsif rising_edge(CLOCK_0)then
            count_0 <= count_0 + 1;
            if count_0 < count_1 then
               led_output <= "1111";
            else
               led_output <= "0000";
            end if;
         end if;
      end process PWM_MODULE_0;

      COUNTER_0: process(RESET,CLOCK_0)
      variable cnt: integer range 0 to 511;
      begin
         if RESET = '1' then
            count_1 <= "0000";
         elsif rising_edge(CLOCK_0) then
            if cnt = 499 then
               count_1 <= count_1 + 1;
               cnt:= cnt + 1;
            elsif cnt = 500 then
               cnt := 0;
            else
               cnt := cnt + 1;
            end if;
         end if;
      end process COUNTER_0;
            LED <= led_output;
end rtl;
```

ADDITIONAL INFORMATION

If you have any questions about the formulas or information found in this document, please feel free to head on over to the forums and ask us some questions!
http://www.pyroelectro.com/forums/viewforum.php?f=26