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Introduction To FPGA And CPLD – Lesson 3: Input and Output

FORMULAS

The following formulas and information are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/input_output/

EXAMPLE QUARTUS II SETUP

The VHDL code for Lesson3 is in the box to the right. It's virtually the same as Lesson2's code except this time we've added an input to the entity port and we're not driving LED_0's output using the BUTTON_0 input singal.

To show that we had complete control over the output signal using the input signal, in Lesson3's video we added a 'not' before the BUTTON_0 in the architecture, which added a hex inverting 'NOT' gate between the input -> output path. The effect of this was that the logic driving LED_0 was effective the opposite of whatever BUTTON_0's input was.

Lesson3.vhd

```
library ieee;
use ieee.std_logic_1164.all;

entity lesson2 is
    port(
    BUTTON_0: in std_logic; -- Pin 23
    LED_0: out std_logic -- Pin 22
    );
end lesson2;

architecture rtl of lesson3 is
begin
    LED_0 <= BUTTON_0;
end rtl;
```

ADDITIONAL INFORMATION

If you have any questions about the formulas or information found in this document, please feel free to head on over to the forums and ask us some questions!
http://www.pyroelectro.com/forums/viewforum.php?f=26