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Introduction To FPGA And CPLD – Lesson 2: Hardware Hello World

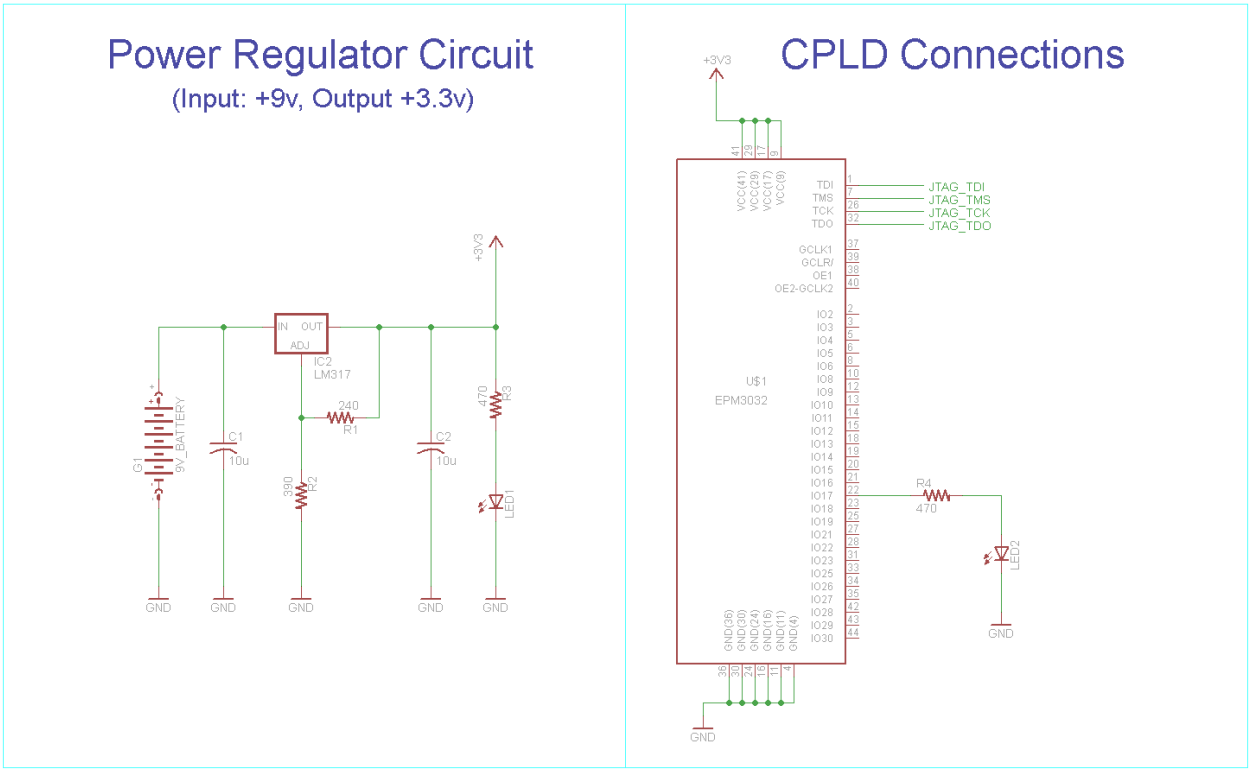
SCHEMATICS

The following schematic material is meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/hello_world/

EXAMPLE SCHEMATIC

In lesson 2 we took a look at how to build a CPLD project that simply controlled whether an LED was on or off. Thus, the hardware schematic didn't need to be terribly complicated.

Below you can see the schematic for lesson 2:



There are only 2 main components to this schematic: the power regulator circuit which takes +9v from a battery and regulates it to +3.3v output which our CPLD will use and the CPLD connections, where power and ground connect as well as the LED off of pin 22. The JTAG signals also need to be connected to the JTAG programmer in order to load the CPLD image.

ADDITIONAL INFORMATION

To ask questions about anything found in this schematic please head on over to the forums located at:
http://www.pyroelectro.com/forums/viewforum.php?f=26