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Introduction To FPGA And CPLD – Lesson 2: Hardware Hello World

FORMULAS

The following formulas and information are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/hello_world/

EXAMPLE QUARTUS II SETUP

The VHDL code for this lesson is short, sweet and to the point (after all its only 13 lines!). The box to the right has the complete VHDL code.

As we discussed in lesson 2, there are 3 parts to this CPLD VHDL code.

[1] The ieee include which allows us to use the standard logic library.

[2] The entity which describes the input and outputs of the system.

[3] The architecture which describes how the system should behave.

Lesson2.vhd

```
library ieee;
use ieee.std_logic_1164.all;

entity lesson2 is
    port(
    LED_0: out std_logic -- Pin 22
    );
end lesson2;

architecture rtl of lesson2 is
begin
    LED_0 <= '0'; -- Output to LED_0
end rtl;
```

ADDITIONAL INFORMATION

If you have any questions about the formulas or information found in this document, please feel free to head on over to the forums and ask us some questions!
http://www.pyroelectro.com/forums/viewforum.php?f=26