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Introduction To FPGA And CPLD – Lesson 4: Combinatorial Logic

SCHEMATICS

The following schematic material is meant to go with the online lesson found here:

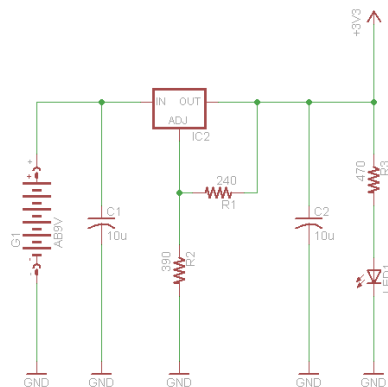
http://www.pyroelectro.com/edu/fpga/combinatorial_logic/

LESSON4 HARDWARE SCHEMATIC

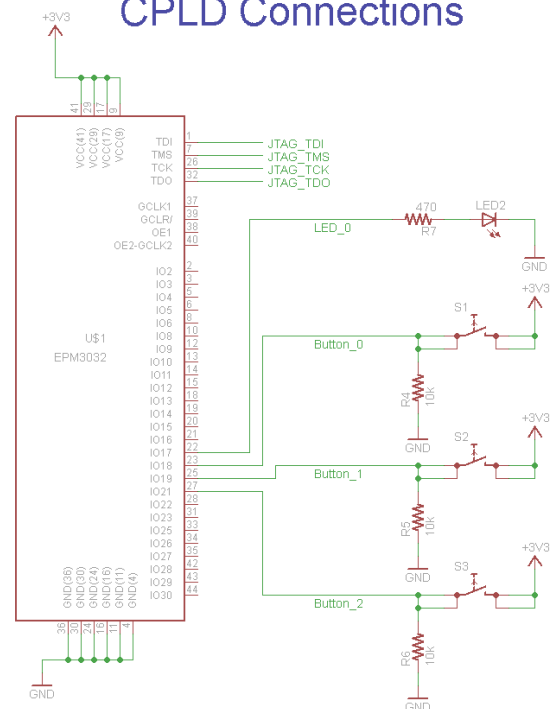
Lesson4 brought the idea of combinatorial logic to the fore-front by implementing a boolean algebra equation with two logic gates. Our CPLD became a discrete logic IC that followed a truth table exactly. Below is the schematic for this lesson:

Power Regulator Circuit

(Input: +9v, Output +3.3v)



CPLD Connections



This schematic shows 3 inputs from push buttons and 1 output to an LED all connected to the CPLD.

ADDITIONAL INFORMATION

To ask questions about anything found in this schematic please head on over to the forums located at:

<http://www.pyroelectro.com/forums/viewforum.php?f=26>