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Introduction To FPGA And CPLD – Lesson 4: Combinatorial Logic

FORMULAS

The following formulas and information are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/combinatorial_logic/

LESSON4 VHDL CODE

The code for lesson 4 can be found to the right. In this code, we use 3 button inputs, all with pull down resistors and an LED for output.

In the architecture we used the translated Boolean algebra equation from the introduction of the lesson to drive the LED output.

Comments were used in the entity declaration to show which pins should be connected to which I/O's on the CPLD.

Lesson4.vhd

```
library ieee;
use ieee.std_logic_1164.all;

entity lesson4 is
    port(
    BUTTON_0: in std_logic; --PIN_23
    BUTTON_1: in std_logic; --PIN_25
    BUTTON_2: in std_logic; --PIN_27
    LED_0: out std_logic    --PIN_22
    );
end lesson4;

architecture rtl of lesson4 is
begin
 --Logic to 'drive' LED_0
 LED_0 <= BUTTON_0 or (BUTTON_1 and BUTTON_2);
end rtl;
```

ADDITIONAL INFORMATION

If you have any questions about the formulas or information found in this document, please feel free to head on over to the forums and ask us some questions!
http://www.pyroelectro.com/forums/viewforum.php?f=26