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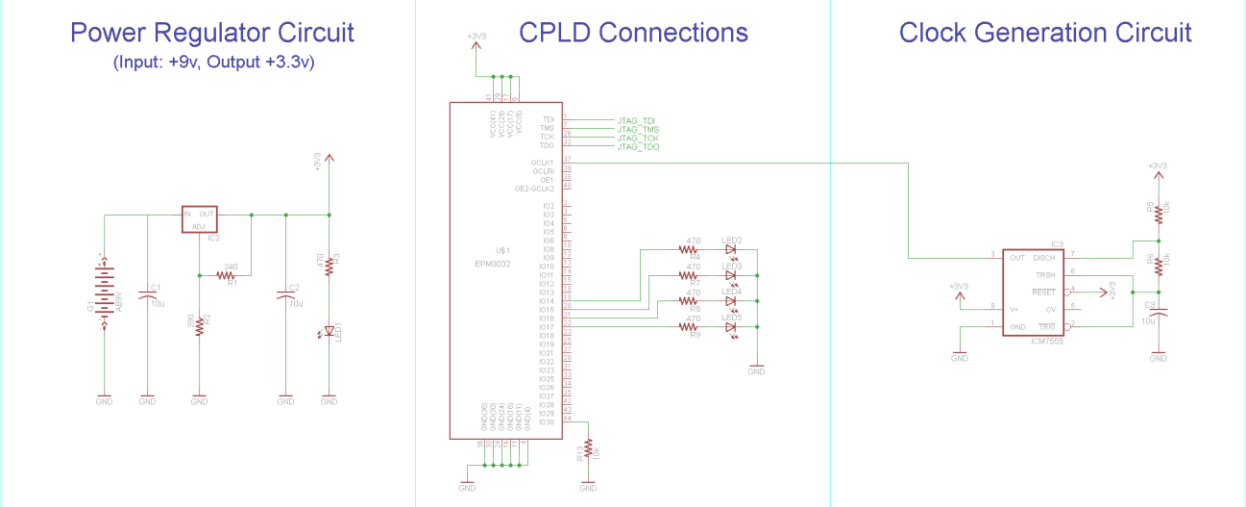
Introduction To FPGA And CPLD – Lesson 6: Design A Binary Timer

SCHEMATICS

The following schematic material is meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/binary_counter/

LESSON6 HARDWARE SCHEMATIC

In lesson 6 we built a circuit using the standard power regulator for a +3.3v output along with a CPLD connected to 4 LEDs with a clock signal at around 10 Hz coming from an ICM7555 timer module. Here's the full schematic:



This schematic is virtually the same as lesson5, but we got rid of the push button and added a few extra LEDs to the mix.

ADDITIONAL INFORMATION

To ask questions about anything found in this schematic please head on over to the forums located at:
http://www.pyroelectro.com/forums/viewforum.php?f=26