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Introduction To FPGA And CPLD – Lesson 6: Design A Binary Counter

HOMEWORK

The following homework questions are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/binary_counter/

The homework for this course will follow a very simple format. Each course will have a homework download for you to do offline and it will consist of 3-5 questions that you should be able to answer if you watched the course.

The questions are not meant to be so challenging as to take you hours to finish, but to stress the more important parts of the lessons and get you thinking about what they mean and how you understand them.

I highly encourage you to post your answers to homework questions in the forums so you can double check that you are getting the right theoretical and practical understanding from the lessons and so that we can start fun conversations about electronics!

HOMEWORK QUESTION 1

What is the difference between the 74HC193 timer/counter module and the one we designed for a CPLD?

HOMEWORK QUESTION 2

Using what you learned in this lesson to build an 8-bit binary counter using VHDL.

HOMEWORK QUESTION 3

Search online to find more information about the library: ieee.std_logic_unsigned.all

Other than using the '+' operator for addition of standard logic, name 2 other functions this library offers us to use.

ADDITIONAL INFORMATION

To get feedback on your homework or to ask additional questions related to this lesson, please post your homework answers or your questions in the online forums at:
http://www.pyroelectro.com/forums/viewforum.php?f=26