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Introduction To FPGA And CPLD – Lesson 6: Design A Binary Timer

FORMULAS

The following formulas and information are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/fpga/binary_timer/

LESSON6 VHDL CODE

In lesson 6 we created a very simple 4 bit binary timer that can count from 0 to 15 based off of a clock input signal.

We used 4 output leds to show the current value of the timer and a clock input signal from an ICM7555 timer module to make the timer count up.

Our clock input was a slow ~10 Hz frequency so its easy to keep track of how things are going visually.

Lesson6.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity lesson6 is
    port(
    RESET:  in std_logic; --PIN_44
    CLOCK:  in std_logic; --PIN_37
    LED:    out std_logic_vector(3 downto 0)
            --PIN 19 to PIN 22
    );
end lesson6;

architecture rtl of lesson6 is

signal count : std_logic_vector(3 downto 0);

begin
    TIMER_0 : process(RESET,CLOCK)
    begin
        if RESET = '1' then
            count <= "0000";
        elsif rising_edge(CLOCK) then
            count <= count + 1;
        end if;

    end process TIMER_0;
    LED <= count;
end rtl;
```

ADDITIONAL INFORMATION

If you have any questions about the formulas or information found in this document, please feel free to head on over to the forums and ask us some questions!
http://www.pyroelectro.com/forums/viewforum.php?f=26