PyroElectro.com - PyroEDU

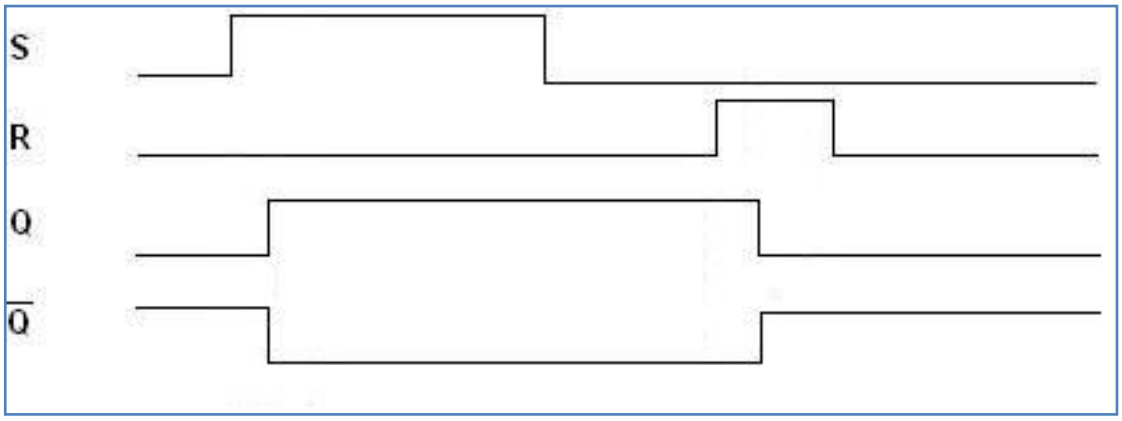
Introduction To Digital Electronics – Lesson 5: The SR Latch

FORMULAS

The following formulas and information are meant to go with the online lesson found here:
http://www.pyroelectro.com/edu/digital/sr_latch/

A BASIC SR LATCH TIMING DIAGRAM

A timing diagram like the one seen below shows the logic levels of the two input signals t the latch: Set and Reset, as well as the two output signals from the latch: Q and Q*. The outputs will react to the input given on the Set and Reset pins.



As you can see above, for a NOR gate SR latch, when the Set signal pulses to logic 1, the Q output sets to logic 1 and the Q* output goes to logic 0. Similarly, when the Reset signal is pulsed with a logic 1, the SR latch resets the Q output to logic 0 and the Q* output to logic 1.

ADDITIONAL INFORMATION

If you have any questions about the formulas or information found in this document, please feel free to head on over to the forums and ask us some questions!
http://www.pyroelectro.com/forums/viewforum.php?f=21